REMARKS

Claims 1-21 are pending in this application.
Claims 8, 11, 17 and 20 are objected to.
Claims 1-7, 9-10, 12-16, 18-19 and 21 are rejected.

In the Office Action dated 25 November 2003, claims 1, 2, 5, 10, 13, 19 and 21 are rejected under 35 USC §102(a) as being anticipated by Bernet et al., and the remaining claims are rejected under 35 USC §103(a) as being unpatentable over Bernet et al. in view of others. These rejections are respectfully traversed.

Claim 1 recites power conversion apparatus comprising a source-side inverter including on/off switches; a drive-side inverter including on/off switches; a dc current link coupled between an output of the source-side inverter and an input of the drive-side inverter; and a controller for operating the source-side inverter in current mode and the drive-side inverter in a commutation mode to achieve sinusoidal input currents at an input of the source-side inverter and sinusoidal output currents at an output of the driver-side inverter.

According to the application, operating the six-switch inverter 18 of Figure 1 in a current mode involves turning on two switches at any given time, whereas operating the six-switch inverter 20 of Figure 1 in a commutation mode involves turning on three switches at any given time (see page 4, lines 7-15).

Bernet et al. disclose a power conversion system 10 including a rectifier 12, an inverter 18, a dc link 44 therebetween, and a controller 22. Both the rectifier 12 and the inverter 18 are "current stiff." At col. 4, lines 35-48, Bernet et al. state that the controller 22 includes a first circuit for controlling the rectifier 12 to control the amplitude of the dc link current and minimize harmonic injection, and a second

circuit for controlling the inverter 18 to create the desired supply conditions for a load. This passage also states that both circuits (12 and 18) are similar, "since four quadrant operation is inherent to current stiff converters."

The office action cites column 5, lines 40-43 and col. 6, lines 10-43 of Bernet et al., However, the passage at column 5 merely states the end results of the controller 22, while the passage at column 6 describes the operation of a generalized "stiff converter" circuit 100. The passage at column 6, which can apply to both the rectifier 12 and the inverter 18, mentions two possible commutation sequences: an active commutation sequence and a passive commutation sequence (lines 35-40). Passive commutation refers to commutation without controlling switching device 82 in the active commutation unit 80 (see col. 12, lines 37-41). Active commutation requires control of the switching devices in a common anode group (col. 12, lines 51-58). Yet these passages do not teach or suggest that the rectifier 12 is operated in current mode while the inverter 18 is operated in commutation mode.

At col. 11, lines 51-54, Bernet et al. state that "[b]ecause both the rectifier 12 and the inverter 18 require similar control of the commutation process, it is sufficient to describe the operation of one of them." In the inverter 18, current modulation is performed, not commutation. Therefore, Bernet et al. do not teach or suggest operating the rectifier 12 in a current mode of operation and the inverter 18 in a commutation mode

Commutation sequences are described at col. 12, line 62+ and Figures 8a-8(g). These sequences are intended to produce switching at zero voltage. In mode 1, switches S5 and S2 are turned on. No current flows, and the DC bus voltage is zero. In mode 1a, only switch S5 is on, and a supply charges capacitors 39-41. In mode 1b, switches S4 and S5 are on, as current flows into the dc link 44 (from the capacitors 39-41). In mode 2, switches S4 and S5 are still on, but

the snubber 82 is turned on. In mode 3, the null vector is commanded, and all switches S1-S6 are turned off. In modes 4 and 5, switches S1 and S2 are on, and current from the supply flows to the dc link 44 (the snubber 82 is on in mode 4 and off in mode 5). Thus Bernet et al.'s controller 22 is concerned with minimizing switching losses in a resonant converter. In mode 1, when the DC bus voltage is zero, switches S2 and S5 are turned on. Switching losses are minimized because the switches S2 and S5 are turned on when the DC bus voltage is zero.

Figures 8a-8g do not disclose a commutation mode as recited in claim 1.

Thus Bernet et al. do not teach or suggest all of the limitations of the power conversion apparatus of claim 1. Moreover, the other documents made of record do not teach or suggest the differences between claim 1 and Bernet et al. Therefore, claim 1 and its dependent claims 9-12 should be allowed over the documents made of record.

Claim 21 recites means for operating a first inverter in current mode and a second inverter in commutation mode to achieve sinusoidal input currents at an input of the first inverter and sinusoidal output currents at an output of the second inverter. Claim 21 should be allowed over the documents made of record for the reasons above.

Claim 2 recites a controller for operating a source-side inverter in current mode and a drive-side inverter in a commutation mode. Therefore, claim 2 and its dependent claims 3-8 should be allowed over the documents made of record.

Claims 2-8 should be allowed for the additional reason that Bernet et al. do not teach or suggest a controller for "commanding the source-side inverter to perform current regulation on the dc current link during a first portion of each

modulating cycle and current mode space vector modulation during a second portion of each modulating cycle."

Claim 13 recites a circuit for commanding a first inverter to perform current regulation on dc current link during a first portion of each modulating cycle and current mode space vector modulation during a second portion of each modulating cycle. Claim 13 also recites that the circuit commands a second inverter to operate in commutation mode. Claim 13 and its dependent claims 14-20 should be allowed because Bernet et al. do not teach or suggest using the rectifier 12 to perform current regulation on the dc link during a portion of the modulation cycle.

The examiner is respectfully requested to withdrawn the rejections and issue a notice of allowability. If any issues remain, the examiner is invited to contact the undersigned.